IN THE CLAIMS

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

9. (canceled)

10. (currently amended) A data processing apparatus adapted for performing scramble processing of transmit data, the data processing apparatus comprising:

a random number generating circuit to generate a random bit data train, said random number generating circuit having a first shift register, a second shift register, and a first adder, said random number generating circuit being arranged such that (i) an output stage of the first shift register is directly coupled to an input stage of the second shift register and to the first adder such that during operation an output from the first shift register is supplied to the input stage of the second shift register and the same output from the first shift register is supplied to an input of the first adder, and (ii) an output

stage of the second shift register is directly coupled to the first adder such that during operation an output of the second shift register is supplied to another input of the first adder;

a data generator to generate bit data of a predetermined pattern and to supply the generated bit data of the predetermined pattern therefrom, said data generator being separate from the random number generating circuit;

a second adder arranged to receive an output of the first adder and the transmit data and being operable to generate scramble-processed data therefrom;

a first switch arranged to receive the scramble-processed data from the second adder and the bit data of the predetermined pattern from the data generator, said first switch being operable to select the bit data of the predetermined pattern at the time of synchronization processing of the transmit data and to select the scramble-processed data when synchronization processing of the transmit data is not performed and to output the data selected.

11. (previously presented) The data processing apparatus according to claim 10, in which the data generator is further arranged to supply the generated bit data of the predetermined pattern to the first shift register and the second shift register, and in which said random number generating circuit is further arranged such that the output of the first adder is supplied to an input stage of the first shift register, and in which the generated bit data of the predetermined pattern supplied to the first switch is the same as the generated bit data of the predetermined pattern supplied to the first shift register and the second shift register.

12. (previously presented) The data processing apparatus according to claim 11, in which the first adder is a modulo 2

adder, and in which the first adder and the second adder are each operable to perform an exclusive-or operation.

13. (previously presented) The data processing apparatus according to claim 10, further comprising a second switch arranged to receive the output of the first adder and the bit data of the predetermined pattern and being operable to output a selected one of the output of the first adder and the bit data of the predetermined pattern to an input stage of the first shift register, and in which the generated bit data of the predetermined pattern supplied to the first switch is the same as the generated bit data of the predetermined pattern supplied to the second switch.

14. (previously presented) The data processing apparatus according to claim 13, in which the first adder is a modulo 2 adder, and in which the first adder and the second adder are each operable to perform an exclusive-or operation.

15. (currently amended) A data processing apparatus adapted for performing scramble processing of transmit data, the data processing apparatus comprising:

a random number generating circuit to generate a random bit data train, said random number generating circuit having a first shift register, a second shift register, and a first adder, said random number generating circuit being arranged such that (i) an output stage of the first shift register is directly coupled to an input stage of the second shift register and to the first adder such that during operation an output from the first shift register is supplied to the input stage of the second shift register and the same output from the first shift register is supplied to an input of the first adder, and (ii) an output stage of the second shift register is directly coupled to the

first adder such that during operation an output of the second shift register is supplied to another input of the first adder;

a data generator to generate bit data of a predetermined pattern and to supply the generated bit data of the predetermined pattern therefrom;

a switch arranged to receive an output of the first adder and the generated bit data of the predetermined pattern, said switch being operable to select the bit data of the predetermined pattern at the time of synchronization processing of the transmit data and to select the output of the first adder when synchronization processing of the transmit data is not performed and to output the data selected; and

a second adder arranged to receive the transmit data and the data selected outputted from the switch and being operable to generate scramble-processed data therefrom.